

BUK9D120-60P

60 V, P-channel Trench MOSFET

9 February 2024

Product data sheet

1. General description

P-channel enhancement mode Field-Effect Transistor (FET) in a leadless medium power DFN2020MD-6 (SOT1220) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- Logic-level compatible
- Extended temperature range $T_j = 175\text{ °C}$
- Side wettable flanks for optical solder inspection
- Small and leadless ultra thin SMD plastic package: 2 x 2 x 0.65 mm
- Trench MOSFET technology
- AEC-Q101 qualified

3. Applications

- Relay driver
- High-speed line driver
- High-side load switch
- Switching circuits

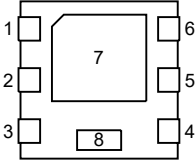
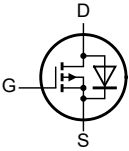
4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j = 25\text{ °C}$	-	-	-60	V
V_{GS}	gate-source voltage		-20	-	20	V
I_D	drain current	$V_{GS} = -10\text{ V}; T_{sp} = 25\text{ °C}$	-	-	-8	A
P_{tot}	total power dissipation	$T_{sp} = 25\text{ °C}$	-	-	15	W
Static characteristics						
R_{DSon}	drain-source on-state resistance	$V_{GS} = -10\text{ V}; I_D = -3\text{ A}; T_j = 25\text{ °C}$	-	95	120	mΩ

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	D	drain	 <p>Transparent top view DFN2020MD-6 (SOT1220)</p>	 <p>017aaa094</p>
2	D	drain		
3	G	gate		
4	S	source		
5	D	drain		
6	D	drain		
7	D	drain		
8	S	source		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK9D120-60P	DFN2020MD-6	plastic, leadless thermal enhanced ultra thin small outline package with side-wettable flanks (SWF); 6 terminals; 0.65 mm pitch; 2 mm x 2 mm x 0.65 mm body	SOT1220

7. Marking

Table 4. Marking codes

Type number	Marking code
BUK9D120-60P	RJ

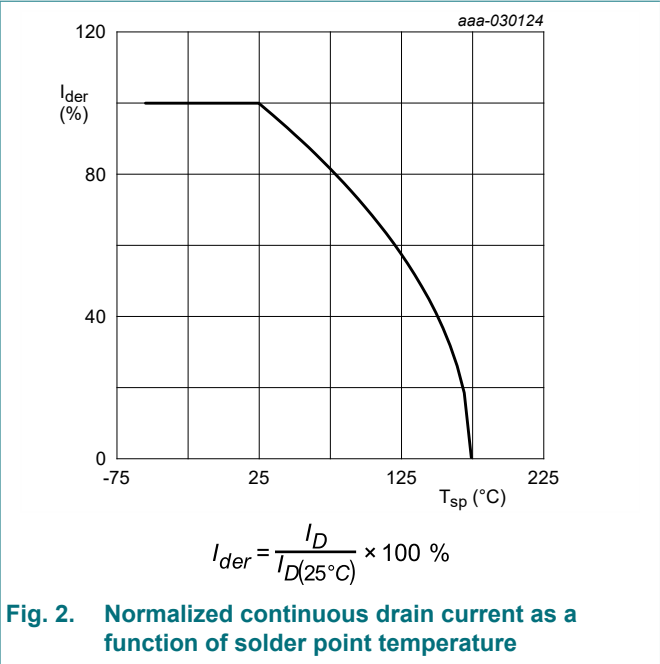
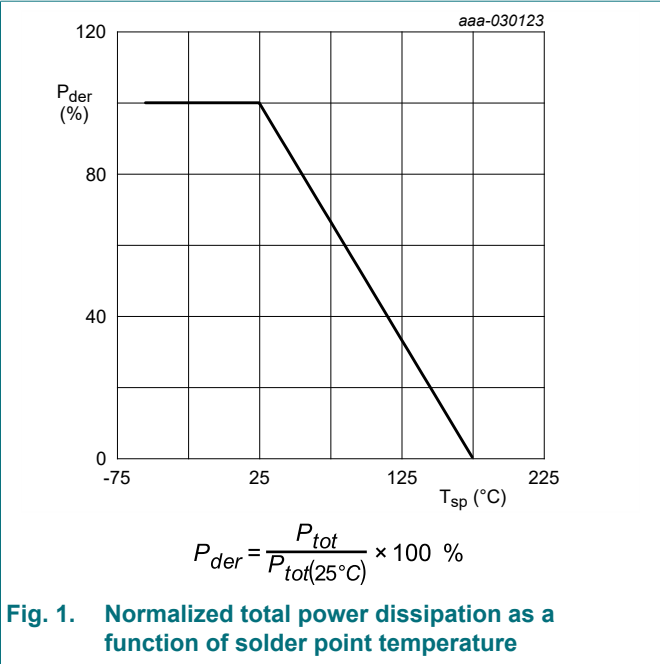
8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{DS}	drain-source voltage	T _j = 25 °C		-	-60	V
V _{GS}	gate-source voltage			-20	20	V
I _D	drain current	V _{GS} = -10 V; T _{sp} = 25 °C		-	-8	A
		V _{GS} = -10 V; T _{sp} = 100 °C		-	-5.1	A
		V _{GS} = -10 V; T _{amb} = 25 °C	[1]	-	-3	A
I _{DM}	peak drain current	T _{sp} = 25 °C; single pulse; t _p ≤ 10 μs		-	-32	A
P _{tot}	total power dissipation	T _{sp} = 25 °C		-	15	W
		T _{amb} = 25 °C	[1]	-	2.3	W
T _j	junction temperature			-55	175	°C
T _{amb}	ambient temperature			-55	175	°C
T _{stg}	storage temperature			-65	175	°C
Source-drain diode						
I _S	source current	T _{sp} = 25 °C		-	-8	A
		T _{amb} = 25 °C	[1]	-	-2.3	A
I _{SM}	peak source current	single pulse; t _p ≤ 10 μs; T _{sp} = 25 °C		-	-32	A
Avalanche ruggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	T _{j(initial)} = 25 °C; I _D = -1.6 A; DUT in avalanche (unclamped)		-	28	mJ

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 6 cm².



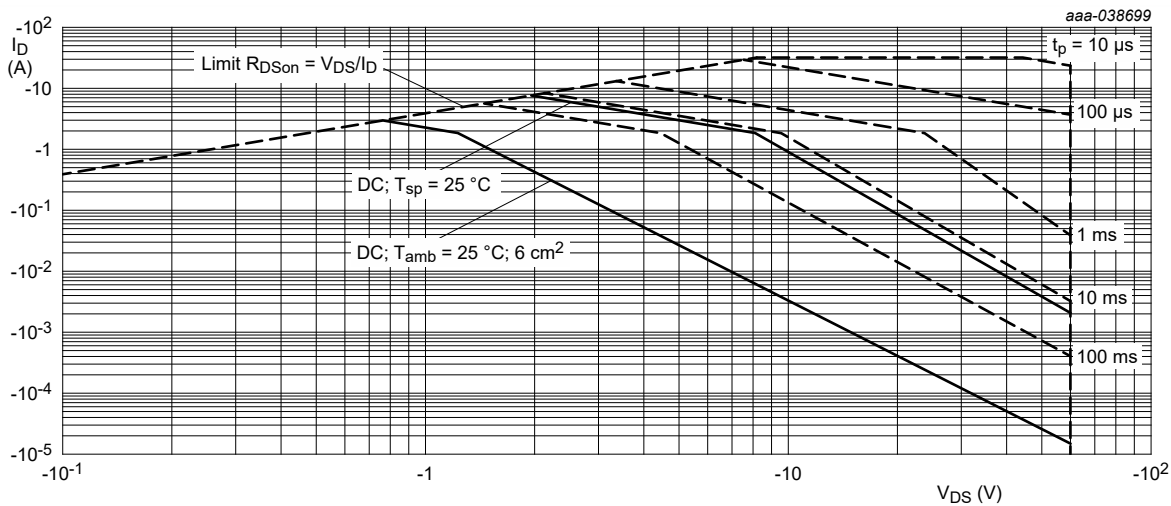


Fig. 3. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	57	66	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	6	10	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 6 cm².

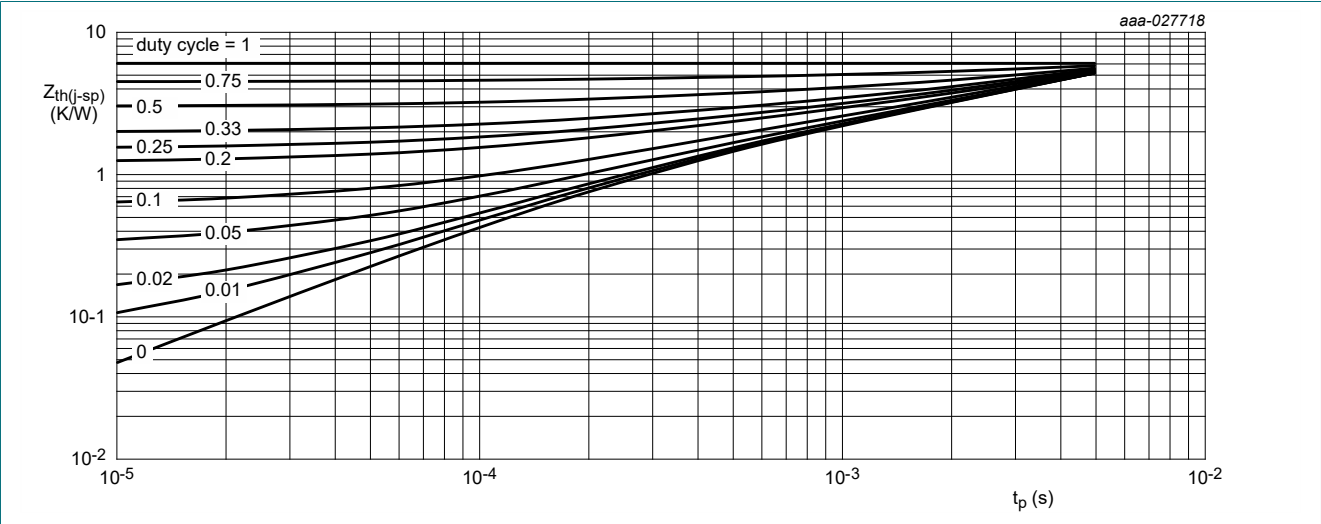


Fig. 4. Transient thermal impedance from junction to solder point as a function of pulse duration; typical values

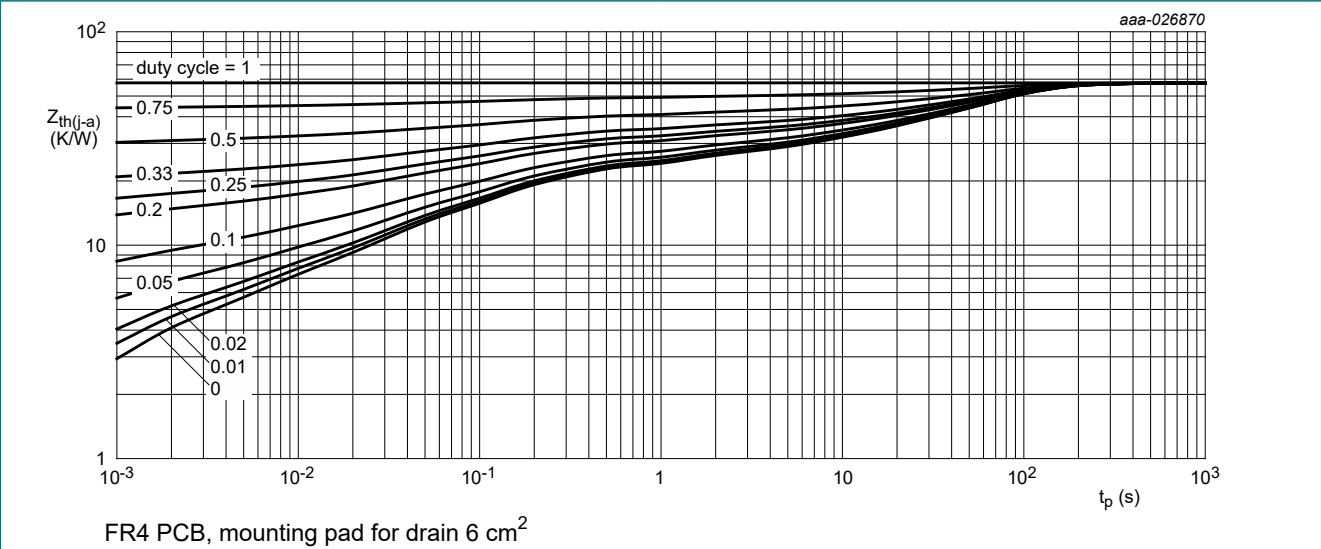


Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
V _{(BR)DSS}	drain-source breakdown voltage	I _D = -250 μA; V _{GS} = 0 V; T _j = 25 °C		-60	-	-	V
V _{GSth}	gate-source threshold voltage	I _D = -250 μA; V _{DS} = V _{GS} ; T _j = 25 °C		-1.5	-2	-2.5	V
I _{DSS}	drain leakage current	V _{DS} = -60 V; V _{GS} = 0 V; T _j = 25 °C		-	-	-1	μA
		V _{DS} = -60 V; V _{GS} = 0 V; T _j = 125 °C		-	-	-20	μA
I _{GSS}	gate leakage current	V _{GS} = -20 V; V _{DS} = 0 V; T _j = 25 °C		-	-	-100	nA
		V _{GS} = 20 V; V _{DS} = 0 V; T _j = 25 °C		-	-	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = -10 V; I _D = -3 A; T _j = 25 °C		-	95	120	mΩ
		V _{GS} = -10 V; I _D = -3 A; T _j = 175 °C		-	202	256	mΩ
		V _{GS} = -4.5 V; I _D = -2.5 A; T _j = 25 °C		-	112	160	mΩ
g _{fs}	forward transconductance	V _{DS} = -10 V; I _D = -3 A; T _j = 25 °C		-	13	-	S
R _G	gate resistance	f = 1 MHz		-	8	-	Ω
Dynamic characteristics							
Q _{G(tot)}	total gate charge	V _{DS} = -30 V; I _D = -3 A; V _{GS} = -10 V; T _j = 25 °C		-	12	18	nC
Q _{GS}	gate-source charge			-	2.1	-	nC
Q _{GD}	gate-drain charge			-	2.4	-	nC
C _{iss}	input capacitance	V _{DS} = -30 V; f = 1 MHz; V _{GS} = 0 V; T _j = 25 °C		-	713	-	pF
C _{oss}	output capacitance			-	48	-	pF
C _{rss}	reverse transfer capacitance			-	27	-	pF
t _{d(on)}	turn-on delay time	V _{DS} = -30 V; I _D = -3 A; V _{GS} = -10 V; R _{G(ext)} = 6 Ω; T _j = 25 °C		-	3	-	ns
t _r	rise time			-	4	-	ns
t _{d(off)}	turn-off delay time			-	24	-	ns
t _f	fall time			-	21	-	ns
Source-drain diode							
V _{SD}	source-drain voltage	I _S = -2.3 A; V _{GS} = 0 V; T _j = 25 °C		-	-0.9	-1.2	V
t _{rr}	reverse recovery time	I _S = -2.3 A; dI _S /dt = 100 A/μs; V _{GS} = 0 V; V _{DS} = -30 V; T _j = 25 °C		-	19	-	ns
Q _r	recovered charge			-	15	-	nC

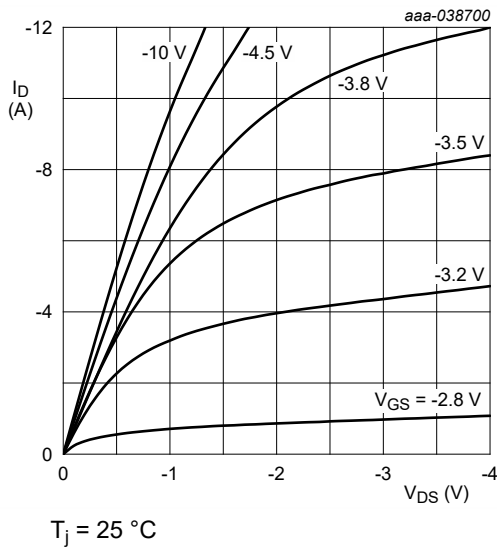


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

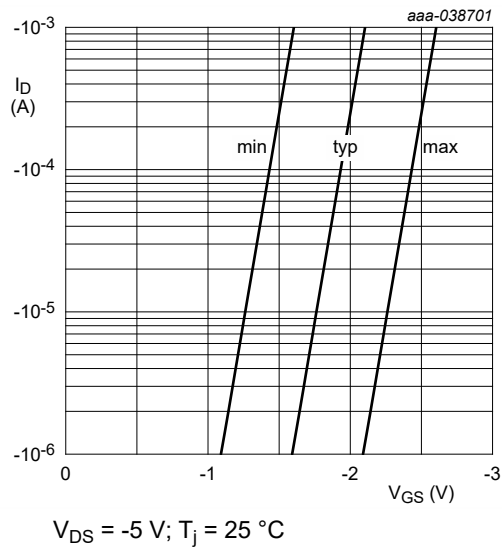


Fig. 7. Sub-threshold drain current as a function of gate-source voltage

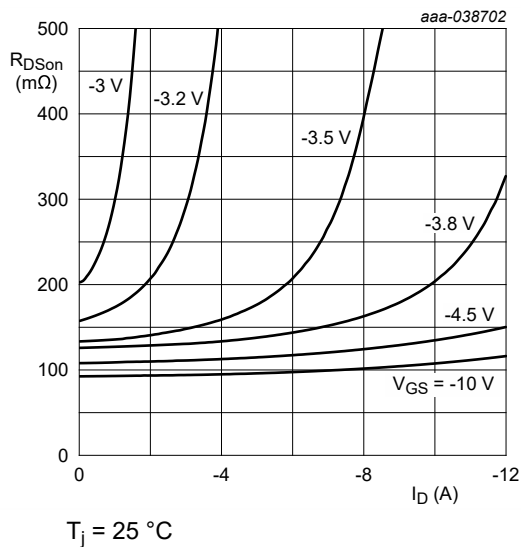


Fig. 8. Drain-source on-state resistance as a function of drain current; typical values

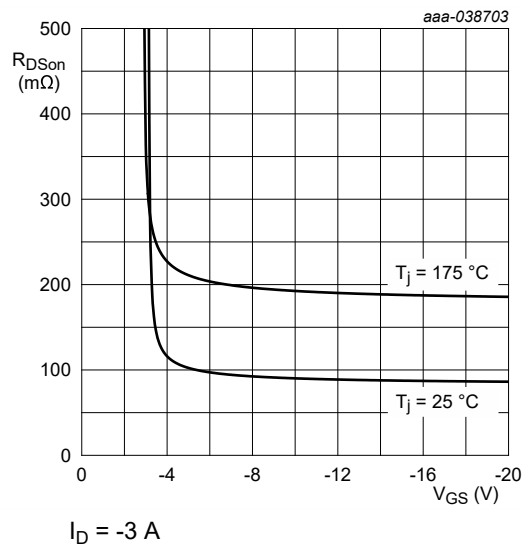


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

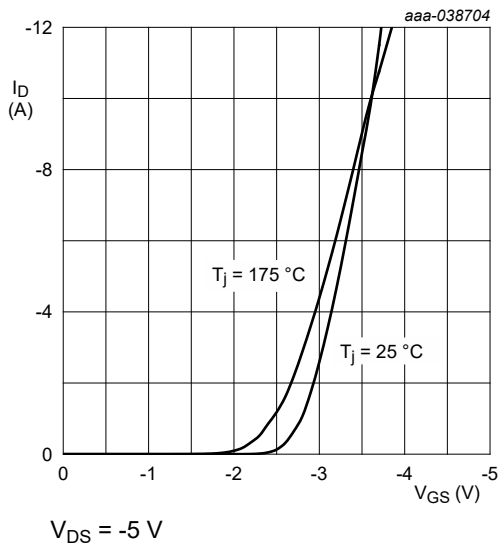


Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

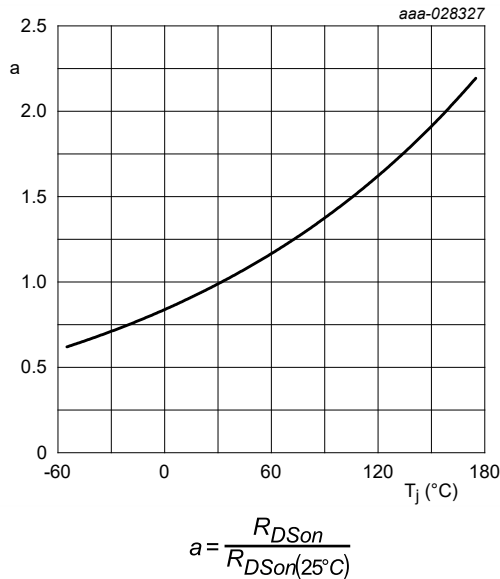


Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values

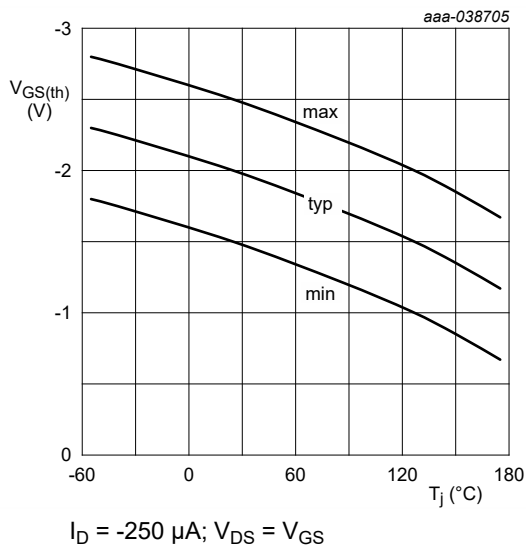


Fig. 12. Gate-source threshold voltage as a function of junction temperature

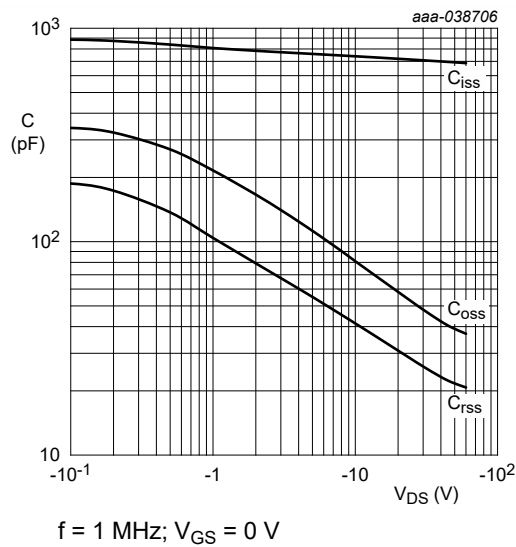


Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

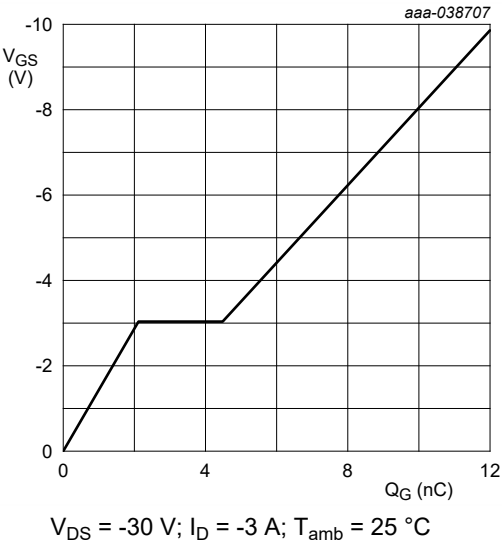


Fig. 14. Gate-source voltage as a function of gate charge; typical values

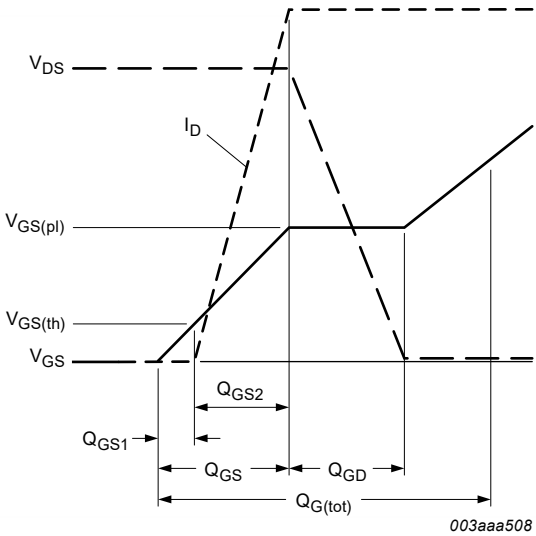


Fig. 15. Gate charge waveform definitions

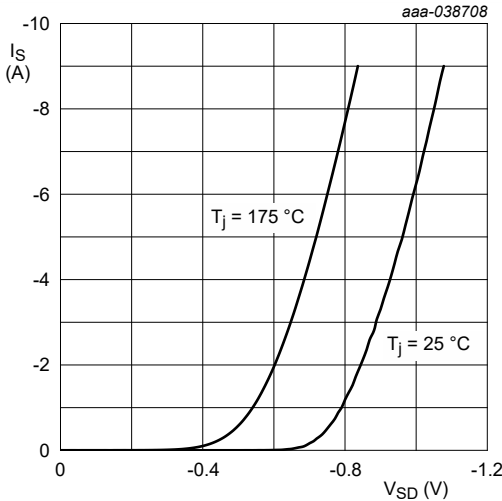
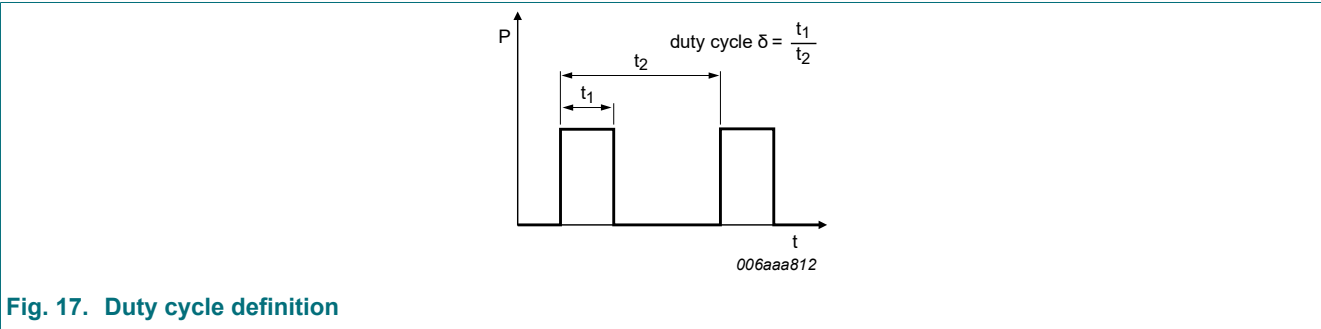


Fig. 16. Source current as a function of source-drain voltage; typical values

11. Test information



Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q101 - Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

12. Package outline

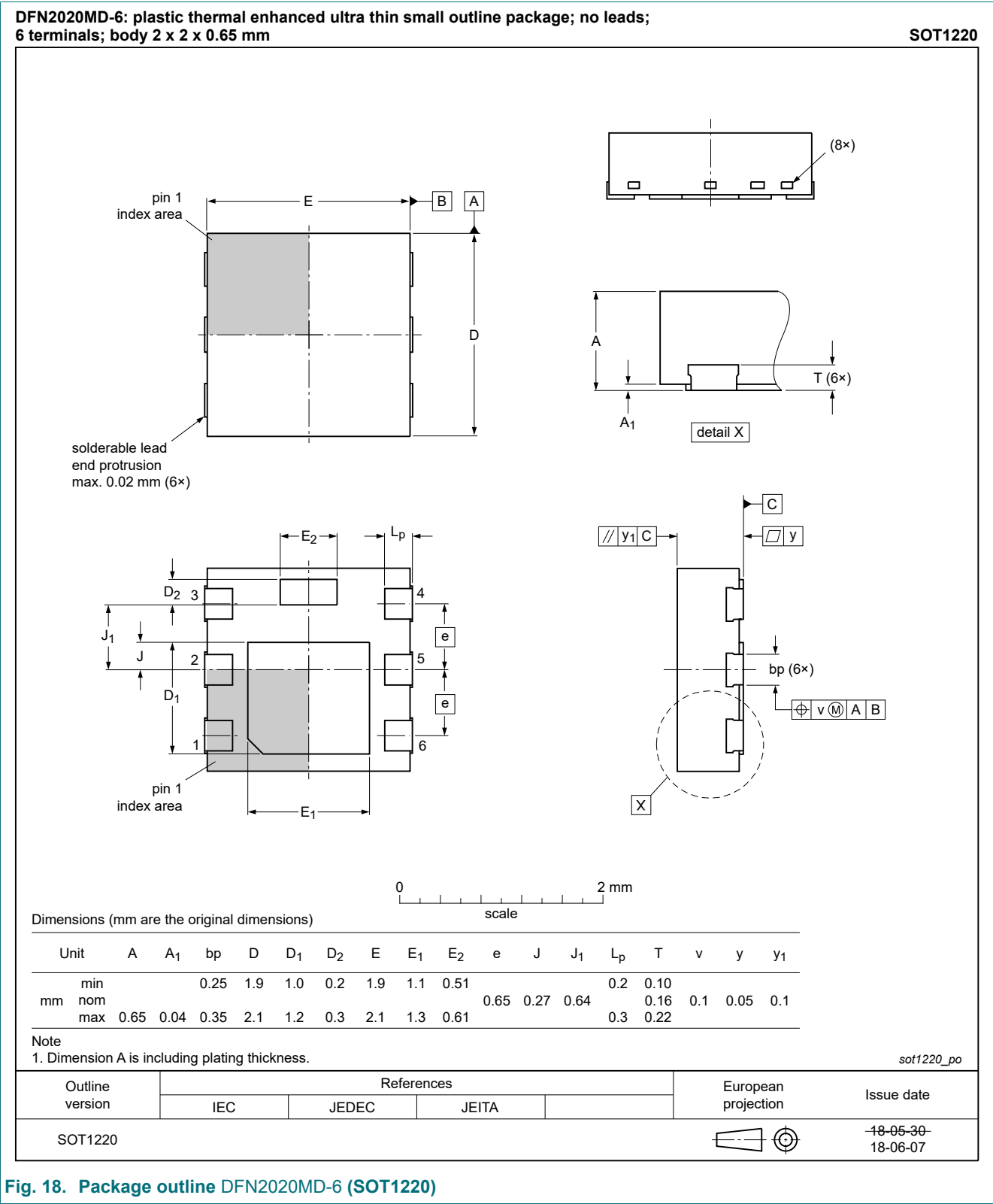
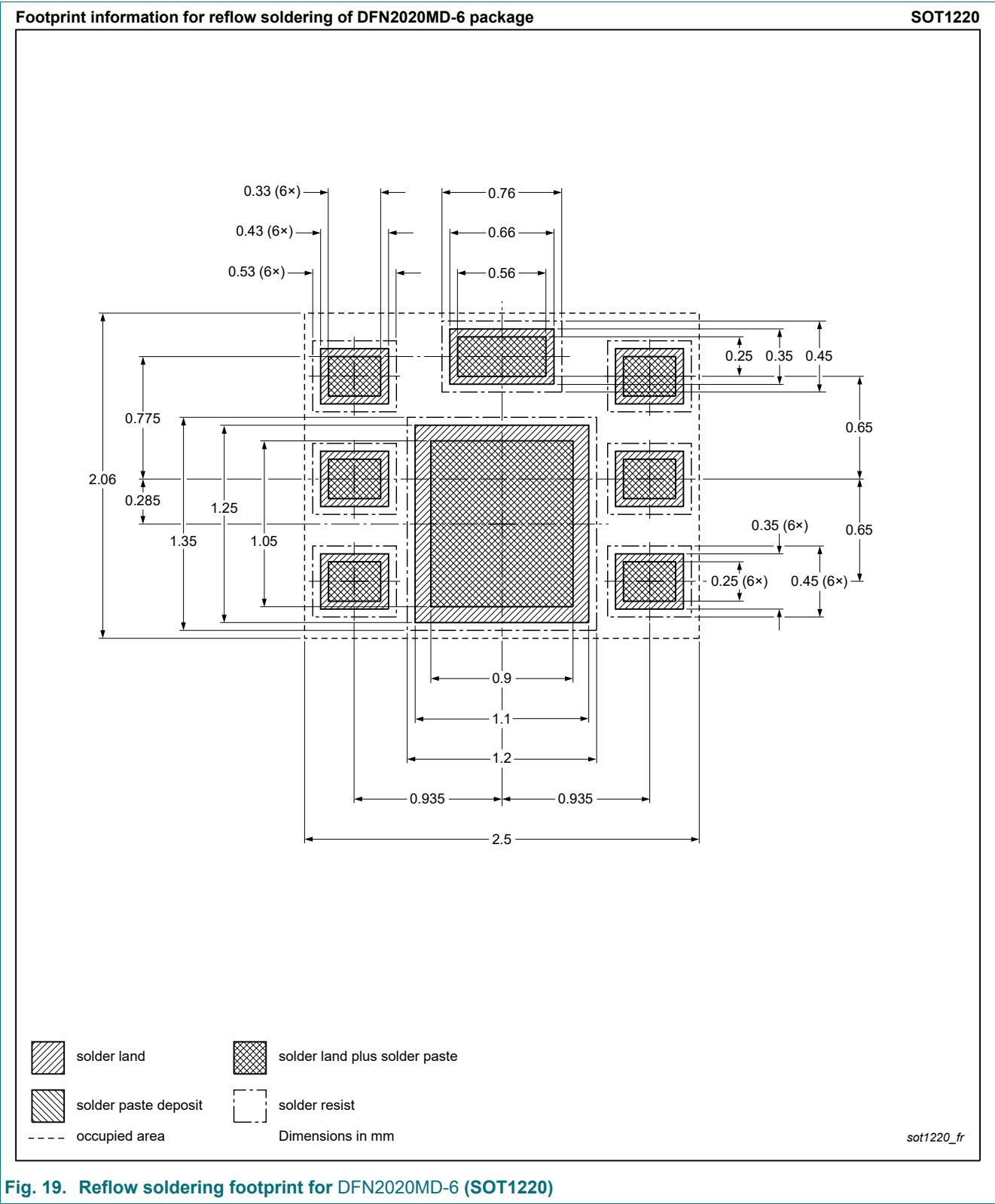


Fig. 18. Package outline DFN2020MD-6 (SOT1220)

13. Soldering



14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
BUK9D120-60P v.1	20240209	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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Contents

1. General description..... 1

2. Features and benefits..... 1

3. Applications..... 1

4. Quick reference data..... 1

5. Pinning information.....2

6. Ordering information.....2

7. Marking.....2

8. Limiting values..... 3

9. Thermal characteristics..... 5

10. Characteristics.....6

11. Test information..... 10

12. Package outline..... 11

13. Soldering..... 12

14. Revision history.....13

15. Legal information.....14

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Date of release: 9 February 2024